Niski CSC 345 Lab – Register Allocation

**Problem 1** – Three Physical Registers

Mapping

r1 → p1

r2 → p2

r3 → p3

r4 → p1

|  |  |
| --- | --- |
| **Virtual Register Code** | **Physical Register Code** |
| load r1, a | load p1, a |
| load r2, b | load p2, b |
| add r1, r2, r3 | add p1, p2, p3 |
| mult r2, r3, r4 | mult p2, p3, p1 |
| print r3 | print p3 |
| print r4 | print p1 |

**Problem 2** – Two Physical Registers

Mapping

r1 → p1

r2 → p2

r3 → p1

r4 → p2

|  |  |
| --- | --- |
| **Virtual Register Code** | **Physical Register Code** |
| load r1, a | load p1, a |
| load r2, b | load p2, b |
| add r1, r2, r3 | add p1, p2, p1 |
| mult r2, r3, r4 | mult p2, p2, p2 |
| print r3 | print p1 |
| print r4 | print p2 |

**Problem 3** – Two Physical Registers and Spilling

Mapping

r1 → p1

r2 → p2

r3 → p2

r4 → p1

|  |  |
| --- | --- |
| **Virtual Register Code** | **Physical Register Code** |
| load r1, a | load p1, a |
| load r2, b | load p2, b |
| add r1, r2, **r3** | add p1, p2, p2 |
|  | store p2, tempVar1 (spill code) |
| load r4, c | load p2, c |
| branchequal r1, r4, tempLabel0 | branchequal p1, p2, tempLabel0 |
| print r1 | Print p1 |
| :tempLabel0 | :tempLabel0 |
|  | load p2, tempVar1 (spill code) |
| print r3 | print p2 |